Scanning Probe Microscopy and Oxidation of Silicon at Breakdown Voltages

Thabo Gcwabaza

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Scanning Probe Microscopy and Oxidation of Silicon at Breakdown Voltages

Thesis submitted to
The Graduate College of
Marshall University

In Partial Fulfillment of the
Requirements for the Degree of
Master of Science

By
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Dr. Michael Norton, Ph.D., Committee
Chairperson
Dr. Robert Morgan, Ph.D.
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Marshall University 2006
The growing importance of Scanning Probe Microscopy (SPM) as a tool for nanofabrication is opening many avenues in lithography nano-science. One type of Scanning Probe Lithography involves electrochemistry at the tip/substrate interface. Atomic Force Microscopy (AFM) with conductive tips and substrates was used in our study to both pattern and image those patterns on silicon substrates. Our long-term objective is to design and fabricate micron-scale patterns of nanometer sized spots on silicon chips that can serve as attachment sites for DNA based nano-arrays. In order to fabricate such substrates a study of the underlying electrochemistry was required. A most promising approach to preparing patterned silicon chips was introduced by the work of Dagata et al., using AFM to locally oxidize silicon surfaces and create controllable nanometer scale features. This thesis reports the determination of the influence of voltage and holding time on oxide growth for three different surfaces, native oxide layers, hydrogen-terminated silicon surfaces, and silicon surfaces functionalized with ultra-thin organic films. Both line and dot patterns were generated at several selected voltages and exposure times. In order to evaluate current efficiency, current was measured during line production. Oxide growth correlates with voltage until it reaches a saturation potential. This saturation appears to be associated with the onset of alternative conduction processes.
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1. Introduction and Background

Overview

The Scanning Probe Microscope (SPM) is of growing importance as a tool in nanoscience. When an SPM is employed to produce patterns on a surface, this is generally termed scanning probe lithography (SPL). One type of SPL involves electrochemistry at the tip/substrate interface. By understanding the chemistry that occurs at this interface, we can exploit and improve these SPL techniques. The scanning probe microscope not only provides the probe that is used to image the surface through a raster scan across the surface, but also to direct oxidation processes which chemically modify the substrate to create nanometer size features. The oxidation process of interest here has acquired many names including nano-oxidation(1), local oxidation(2,1), anodization (3,15), AFM- assisted surface oxidation and direct oxidation(4). However, before all these names were proposed by other groups, Dagata was the first to report the use of the proximal probes to locally oxidize the Silicon surface in 1990 (5). Use of SPM in the manipulation of matter and in the identification of size, shape, and composition of sub-micrometer molecular structures is growing and becoming an accepted method in the field of science and industry (6). Significant effort is being directed toward the understanding of the substrate and the production of instrumentation necessary for the manipulation and the formation of nanostructures.
There are many new devices that require development of nano-scale patterning and machining systems. The design of devices at the nanometer-scale has provided challenges and opportunities for many researchers in the biological and chemical fields. Nano-sensors serve as one of the example target technologies making their way to the market, but the growing nanotechnology field has more to offer. There are many more example areas that will make use of this study. Working with very small bits of material (nanometer depths at a surface) is difficult because these objects are hard to push around or manipulate. Also, as compared to bulk materials, the characteristic behavior of matter can change at the small size scale, so that surface and quantum confinement phenomena become more important than bulk electro/mechanical properties. Advances in the development of instrumentation for surface studies, specifically the invention of scanning probe microscopy (SPM), has opened up challenging opportunities for the surface modification of metals, semiconductors and polymer materials (6). SPM is a class of instrumentation that is used for imaging, characterization and surface manipulation of material structures at atomic to nanometer scale which is the scale that interests most scientists working and sharing the ideas and interests within the nano-science field. The SPM family of instruments includes the Atomic Force Microscope (AFM), which is used for this thesis. As indicated by the name, the SPM uses an electro-mechanical probe as the proximal imaging tool, as compared to conventional microscopes where a lens and detector are used (6). The type of measured interaction of the probe with the substrate or surface defines what type of microscope within the SPM family is to be used. AFM is further described below. Local anodic oxidation using AFM is the
primary technique utilized in this thesis study. Local anodic oxidation using AFM as the process of forming angstrom to nanometer oxides on metals or semiconductor surfaces has a significant history (2,4,5,7,8,14,15). The process of oxide growth on silicon is termed anodization. Oxidation is the loss of electrons while the gaining of electrons is reduction (9). The behavior of silicon in this system is related to electron transfer from an electrode to an electrolyte and then ionic transfer from that electrolyte to the Si surface. This study has its beginnings in traditional electrochemistry, where an electrode/electrolyte interface is the system of interest. Silicon is the substrate that is oxidized while water contributes as the electrolyte and as a reactant in the system. In this thesis, I investigated the local anodic oxidation of silicon to silicon dioxide using the AFM. The determinations of the height and width of SiO₂ produced by applying several bias voltages provides some insight into the limitations of electrochemical lithography. Electrochemical SPL is a complex process, and several parameters contribute in the formation of nanometer anodic oxide features on the semiconductor surface. Bias potential, dwell time and current parameters were evaluated to determine how they influence and affect the growth of anodic oxide on different surfaces, including silicon with its native oxide, the hydrogen terminated surface of silicon and silicon with an organic monolayer. One way in which this work can be distinguished from that of others in the field is that most of the lithography was performed in a high current (µamp) regime that has been called ‘not possible’ (Dagata, personal correspondence) and ‘anomalous current’ (4). The work presented here was carried
The Trend Toward Miniaturization

Miniaturization of electrical devices has been a persistent goal and challenge to the electronic industries and within the field of nano-science. In 1947 and in 1971, two of the most important inventions were generated, the invention of the transistor and the microprocessor, respectively (10). The invention of these devices has improved the world, by enabling electronic devices to be much smaller than was previously possible. Miniaturization of devices has made it possible the majority of us to own pocket-size electronic phones, desktop computers and even laptop computers which would have been impossible without these inventions because of size and cost factors (10). Understanding of the transistor requires some education or knowledge in physics and chemistry, and has attracted many to the field of nano-science. The basic ideas are fairly simple according to (10). “Transistors are based on solid substances known as semiconductors”. Silicon which is the center of this study, is a semiconductor which has been the core material of the semiconductor industry. Producing and controlling the flow of electrons within this material is the most important consideration in designing solid state electronics.

Conduction in Semiconductors

Electrons in an ideal crystal can only have certain energies. They can occupy called allowed bands. There are also un-allowed energies which fall within the
band gap. Since there are no energy level to be occupied, normally no electrons exist at these energies (8). The electronic properties of a semiconductor can vary depending on the presence of impurities. Impurities in semiconductors can serve as donors or acceptors of electrons to modify the conductivity of the semiconductor. The width of the band gap in a material determines whether a material is able to conduct readily or not. Metals have overlapping of the valence band with conduction band, thus electrons are able to migrate from band to band (10). In semiconductor materials like silicon, the band gap is narrow and electrons can be excited from the valence band to the conduction band (10). In the case of an insulator, the band gap is wider, thus making it difficult for electrons to jump from the valence band to the conduction band. In an intrinsic (pure) semiconductor the band that is mostly filled with electrons is called the valence band and the mostly empty bands at higher energy are called conduction bands (8). The energy gap between the two bands is called the band gap. At room temperature, electrons are mostly in the valence band. One can add heat and the electrons can be thermally excited from the valence band to the conduction band, thus creating holes in the valence band (17,3). In the presence of an electric field these holes are said to behave like particles (11). Some excited electrons loose their energy and return back to the valence band while others become excited, maintaining an equilibrium. When current is passed the electrons excited to the conduction band can move in one direction, while holes moves in the opposite direction, and we thus say electrical conduction is due to motion in both directions (3). The Fermi level, the highest energy level occupied by electrons at zero Kelvin, exists in the band gap.
and varies based on the amount and type of dopant or impurities present in a doped (extrinsic) semiconductor. The Fermi level is described as the electrochemical potential of electrons (8). The introduction of different types of impurities in a semiconductor influences the electronic properties. There are two types of extrinsic semi-conducting silicon, $n$-type silicon, and $p$-type. $n$-type silicon is doped with elements that lead to the donation of electrons to the silicon conduction band, for example phosphorous. The $p$-type refers to the silicon doped with acceptors (elements accepting electrons from valence band), for example boron. Silicon is prepared for use in the semiconductor industry by growing it into crystals with a specific orientation. Important to our understanding of silicon is the terminology of the types of silicon crystal orientation. When silicon is grown as a single ingot crystal, it is cut into wafers with a specific orientation, which depends on how the cut plane intercepts the crystallographic directions. The material used in this study is $p$-type silicon with $<100>$ orientation. As described below, this orientation leaves two dangling bonds on each atom on the face of the wafer. As purchased, silicon always has a layer of SiO$_2$ on the surface, which is called the native oxide. For our study it is important to adopt a procedure for removing this layer in order to prepare surfaces of technological interest.

**Motivation for This Project: Norton Group Nano-architectures Project**

One of the goals of the work progressing in the Norton lab is to design and improve surface based molecular sensors. The Norton laboratory has long and short term goals related to the design and production of immobilized DNA on substrates. The
DNA to be immobilized first is called a DNA director strand, which is 1 um in length. The binding of DNA building blocks (named block A and block B) is represented in Figure 1.1. The concept is to grow large structures consisting of these building blocks on top of the DNA director strand, which serves as a scaffold to direct the growth of a nanostructure. The DNA director strand is labeled with functional groups that will serve to bond the molecule at specific locations on the surface of the substrate. One approach intend to provide a binding mechanism to gold spots is to synthesize thiol modified DNA primers which are about 25 base pairs in length, which are complimentary to one end of the director strand. On the other side of the director strand the primers are modified with iso-cyanide to promote binding to platinum on the substrate surface.

**Figure 1.1**: (a) Illustrates the design of the director strand. (b) illustrates the steps necessary to produce complex architectures on the surface, starting with attachment of the director strand to the surface of a substrate chip.
In Figure 1.1(a) the design of the director strand, including its binding sites is illustrated. There is a thiolated primer complimentary to the director strand on one end and on the other end there is a primer labeled with iso-cyanide. Thiols bind with gold, while iso-cyanide binds with platinum. Both endings are designed to bind to metal sites on a substrate surface. There is also a region for the DNA building blocks to grow, called the 6 repeat region. Figure 1.1(b) Shows a stepwise method which begins with an isolated metallic site on the chip surface will bind the one dimensional director strand, followed by the attachment of DNA building block (red), then DNA building block (blue). This process is repeated until growth is completed.

The direction in this thesis has been driven by the Norton group project, and also several authors that have guided my understanding of the manipulation of matter. The goal was to fabricate arrays of metallic spots which would serve as attachment sites for DNA director strands with the longer range goal to design and produce surface localized complex nanostructures containing very rare custom synthesized organic/inorganic molecules, using stepwise or sequential assembly (12). The objective was set before this thesis was begun. Two of the former students in the group have successfully completed synthesizing director single strand which has 6 repeats to enable nucleated growth of both A and B DNA building blocks. An immobilized director strand will provide regions of DNA sequential growth, and is termed 6 repeats as seen in the figure 1.1b The focus of this work was to fabricate substrates with two different metal sites of attachment, consisting of gold and
platinum. But before this goal could be achieved a reproducible method of creating regions for depositing metals on silicon substrates had to be devised. This study will be reports the patterning steps necessary for the preparation of a silicon substrate that can be further processed through the deposition of metals. The method selected for patterning the silicon surface was anodization, using AFM.

**Project Outline**

The following is an outline of the experiments performed in this study. The remainder of the introduction is arranged to provide a foundation for understanding the materials, methods, results and discussion to follow.

- Preparing ultra-clean surfaces using standard industrial techniques.
- Preparing atomically flat hydrogen terminated surfaces
- Preparing silicon with a grafted organic monolayer.
- Using the AFM to locally oxidize three different types of surfaces, native oxide, hydrogen terminated and organic terminated silicon. This involves setting up well defined, well controlled experiments to investigate nano-electrochemistry.
- Pattern surfaces to create sites suitable for gold deposition.

**Preliminary Studies: Attempted Gold Patterning Led to Anodic Oxidation**

A first approach to achieve gold deposition at nanometer scale utilized a method adopted from Sumio Hosaka’s paper (13). In that paper Hosaka addressed both
theoretically and experimentally the feasibility of making nanometer-sized dots on an insulator by field evaporation (formed on a natural SiO$_2$/Si substrate) using an AFM. The idea was to make nanometer size gold dots on silicon with native oxide (SiO$_2$/Si), using the Atomic Force Microscope. Field evaporation is the phenomena in which atoms are ionized at the presence of an extremely high electric field of the order of a few V/nm. Such high electric fields can be achieved and controlled by applying relatively low voltages to an AFM cantilever. When voltage is applied, the atoms start to ionize and evaporation begins. The results obtained in similar experiments performed at Marshall looked promising as an array of spots was observed on the silicon substrate. A chemical method was needed to characterize the surface in order to determine whether gold was deposited at the specific areas as anticipated. A more careful review of literature revealed that the Hosaka group (10) had not confirmed the nature of the material they had deposited.

The wet chemistry method of silver enhancement on gold was performed under the light microscope to determine whether the spots were actually gold, monitoring the Ag reaction as it progressed by looking for clusters of black silver oxide as it formed. Using the energy dispersive mapping capability of the Scanning Electron Microscope to map the surface distribution of silver, the expected array of silver spots was not observed. It was concluded that the array of spots was not composed of gold. As a further test, a substrate was cleaned by RCA methods (see methods section) then re-patterned using the same gold cantilever and changing no parameters. The same array of dots seen in the first attempt was again observed in this experiment. Silver enhancement was performed to enlarge the putative gold
spots, again the silver enhancement method appeared to be too non-specifically active to demonstrate any success in gold patterning. As another test, the experiment was modified, replacing the gold coated cantilever (proximal probe) with a Si$_3$N$_4$ cantilever. With surprising result, an array of dots was seen again, evidence that these could not be gold spots. It was concluded that rather than depositing gold, the experiments led to locally oxidizing the surface of silicon. A short additional literature search led to Dagata’s papers which propose local oxidation of silicon with the use of proximal probes to fabricate nanometer scale oxide features (5).

**Patterning Silicon via Local Anodic Oxidation**

In contrast to bulk chemistry which occurs in well mixed solutions or gas mixtures, electrochemistry occurs at the interfaces (or inter-phases) that are present at electrode surfaces. These electrode surfaces are usually considered as the junction between the ionic current that occurs in electrolyte solutions (such as water) and the electronic current that occurs in metallic circuits (9). As will be seen, electronic current can also flow through water with high enough voltages and field strength. The type of chemical transformation that is of relevance for this thesis work is usually called electrolytic (that is, electrical energy is used to achieve chemical changes) in contrast with a galvanic processes which use chemical change to generate electrical energy (9). In both galvanic and electrolytic cells, an electrode and electrolyte is required to have charges transferred in the interface. The transfer of electrons causes oxidation and reduction at the electrodes of electrochemical
cells (9). The electrochemical AFM system used here consists of a negatively biased conductive silicon tip and the positively biased silicon substrate. An example of a conventional electrolytic cell is presented in Figure 1.2a, consisting of two platinum electrodes in a water based electrolytic medium. The electric field is relatively low for the conventional cell compared to the high electric field in the AFM system (illustrated in Figure 1.2b). The high field is created by applying voltage between electrodes which are extremely close together. As an illustration, consider the application of a potential across water the water bridge accumulated at the tip substrate gap through capillary forces from the ambient humidity, as seen in Figure 1.2b. If one applies a 10 volt potential and assumes that the separation of the electrodes in Figure 1.2b is 0.1nm, then a field strength of 1,000,000,000 V/cm will be present. This field strength is much higher than that which exists in conventional electrochemical systems, so it may not be surprising to find that the system behaves differently than a traditional electrochemical cell.
Two different anodic oxide growth mechanisms have been proposed in the literature (4).

1 - Faradaic oxidation with strictly ionic current.

2 - High fields limit, which leads to water ionization and high ionic/electronic current.

Dagata and other groups have described the current observed when directly oxidizing the silicon substrate in a low current, pico- and nanoamp regime (2,14).

The studies reported here have been conducted in the region which Lyuksyutov describes as the high current regime (4), where the current readings are in the microamp range. A short review of these regimes is presented below.
1- Low current procedures

When a voltage is applied to the tip-silicon interface, a high electric field is created. The presence of the field grows a stable meniscus of water between the tip and the substrate and thus a water bridge forms. The bridge acts as an electrolytic medium. When a voltage is applied, current passes, and in the substrate charges are transported by the electrons while at the electrolyte the movement of ions is responsible for the charge transportation. Charge transfer is explained in terms of two half reactions occurring near the tip, and at the silicon surface. The charge passing at this electrode-interface when current is passing is known as faradaic current and is associated with the low current regime. It is responsible for the oxidation of the substrate. Dagata (5) was the first to demonstrate local anodic oxidation in 1994. In his explanation the anodic current is carried by the oxyanions which carry the charge while the field assists in transporting these oxyanions through the growing oxide to react with the holes in Si or $h^+$ (7).

Below are some of the electrochemical reactions considered to be active in the low current regime. Although the stated half reaction may differ in terms of holes or electrons involved, the balanced net reactions are the same.
Reactions From Avouris and Dagata (15)

<table>
<thead>
<tr>
<th>Electrochemical ½ reactions near the tip</th>
<th>Not described but presumed to involve production of H₂ gas</th>
</tr>
</thead>
<tbody>
<tr>
<td>½ Reaction at the silicon:</td>
<td>Si + 4h⁺ + 2OH⁻ → SiO₂ + 2H⁺</td>
</tr>
<tr>
<td>The net electrochemical reaction (presumed):</td>
<td>Si + 2H₂O → SiO₂ + 2H₂↑</td>
</tr>
</tbody>
</table>

2-High current regime

Lyukstutov’s anomalous current result (4) is consistent with the results observed in the experiments described below in this thesis. They were performed in the high current regime, where currents in the micro amp range were observed. His explanation of the high current regime is that the electrons from the Fermi level of the tip ionizes water and thus produces more than the typical ionic species in the electrolyte. “The high current is related to an electrical breakdown resulting in conduction dominated by electrons rather than ions” (4). Below are reactions that he uses to explain this high current breakdown (see Figure 1.3).
Field-induced ionization of water molecules yielding electrons, protons, and free radicals (OH·) as follows:

\[ \text{H}_2\text{O} \rightarrow \text{e}^- + \text{OH}^- + \text{H}^+ \]

Number of options for OH· consumption:

\[ \text{OH}^- + \text{OH}^- = \text{H}_2\text{O}_2, \]
\[ \text{OH}^- + \text{H}^- = \text{H}_2\text{O} \]
\[ \text{e}^- + \text{OH}^- = \text{OH}^- \]

**Figure 1.3:** Schematic representation of the tip-surface junction and the species present at breakdown, according to Lyuksyutov, in the high current regime, in the electrolyte(4).
The excess e\(^-\) travel through the Si substrate, and their number (current) is related to the voltage through ohms law (4). Finally Lyuksyutov et al. mention that avalanche type breakdown occurs in both the silicon space charge region and in the meniscus (4), and thus causes high current to flow in the conduction band. Zhang also describes avalanche breakdown in semiconductor systems. In his description the free carriers in the space charge region in, in the presence of a sufficiently high electric field, gain enough kinetic energy to break the covalent bonds in the lattice through inelastic collisions, thus creating more carriers (8). The reactions at the electrodes are not dissimilar to those suggested by Avouris and Dagata listed above. The major difference is that high electronic currents are possible above breakdown voltages.

**Reactions From Lyuksyutov (4)**

<table>
<thead>
<tr>
<th>Electrochemical ½ reactions near the tip</th>
<th>2H(_2)O + 2e(^-) → H(_2)↑ + 2OH(^-)</th>
</tr>
</thead>
<tbody>
<tr>
<td>½ Reaction at the silicon:</td>
<td>Si + 2OH(^-) - 4e(^-) → SiO(_2) + 2H(^+)</td>
</tr>
<tr>
<td>The net electrochemical reaction</td>
<td>Si + 2H(_2)O → SiO(_2) + 2H(_2)↑</td>
</tr>
</tbody>
</table>

The net reactions must be the same as one would observe at reduced potentials, in bulk solution experiments.
Reactions from T. Gcwabaza

<table>
<thead>
<tr>
<th>Electrochemical $\frac{1}{2}$ reactions near the tip</th>
<th>$4e^- + 4H^+ \rightarrow 2H_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\frac{1}{2}$ Reaction at the silicon:</td>
<td>$2H_2O + Si \rightarrow SiO_2 + 4H^+ + 4e^-$</td>
</tr>
<tr>
<td>The net electrochemical reaction</td>
<td>$Si + 2H_2O \rightarrow SiO_2 + 2H_2\uparrow$</td>
</tr>
</tbody>
</table>

Properties of silicon and its oxide

The principal raw materials that we have used in this work are crystalline silicon and its oxide, silicon dioxide, that forms on the surface of this material. This thin oxide layer is known as native oxide and grows as a result of the oxygen and water found in typical ambient (surrounding) conditions (8). Some relevant properties of Si and Si oxide are discussed below.

Figure 1.4: Representation of unit cell of silicon (8).
Silicon is an element with a diamond lattice structure in which the silicon atoms are $sp^3$ hybridized. Figure 2.1 presents the crystal structure of silicon. Table 1.1 lists some physical properties of an ideal Si crystal. The intrinsic conductivity of the silicon is $4.3 \times 10^{-6} \ \Omega^{-1} \text{cm}^{-1}$, and a band gap of 1.12 eV at 300k (8, pg 45). Each silicon atom exhibits four bonds in a tetrahedral $sp^3$ arrangement, with angles of 109.47 degrees. Silicon used in experiments and in semiconductor industries is usually doped with foreign atoms as discussed above. Common types of donors for silicon are P, As, and Sb, while the acceptors are B, Al, and Ga. The silicon used as substrates in these studies was doped with boron ($p$-type Silicon), and had a 0.1 – 0.3 $\Omega \text{cm}$ resistivity. A doping level of $10^{16}$-$10^{17} \text{ cm}^{-3}$ can be inferred, based on table 1.2 taken from Zhang’s book (8, pg 47, ref 27).
Table 1.2: Resistivity versus doping concentration of silicon at 23° (8)

All the experiments presented here were conducted using $p$-type, boron doped silicon substrates with $<100>$ orientation, even though we had performed other studies on different surfaces such as mica and graphite. A diagram and STM image of this arrangement can be seen below in Figure 1.5. According to Zhang et. al (8), at this crystal surface, some atoms will have orbitals “dangling“ in the vacuum, i.e. $sp^3$ orbitals with lone electrons (which is the result of the cleavage of the silicon bulk) which are highly reactive. These orbital are normally referred to as dangling bonds (for $<100>$, see Figure. 1.4 b and c). Silicon as a result reacts more readily with air forming a thin oxide surface layer (8). In appropriate environments, silicon can be terminated with hydrogen, fluorine, oxide and hydroxyl groups (8). In these studies the native oxide will be removed, forming a hydrogen terminated surface, which will be locally oxidized with proximal probes(2,15,4,5,16,14,7,17,18,8). To remove possible contamination of the surface of the silicon with metallic, organic or even ceramic species (8), the methods from RCA (Radio Corp. of America) will be employed. This cleaning process and the production of the hydrogen terminated
surface is expected to increase the conductivity of the surface during the interaction with the electrolyte when anodizing the silicon surface. The experiment result thus will be influenced by the methods of cleaning, exposure of the hydrogen-terminated surfaces to air and to light, doping concentration and local distribution and type of dopants in the silicon, among others. To reduce the surface energy, the silicon surface re-organizes, thereby decreasing the number of dangling bonds. Dangling bond densities and positions, and thus of the surface reconstruction, will depend upon crystal orientation as well as the temperature and kinetics of the system (8).

Figure 1.5: Representation of Si <100> (a) unit cell structure (b) diagram of the surface of an unreconstructed <100> cut Si crystal and (c) STM image of a clean Si <100> surface, larger steps in surface indicate mis-cut by 4 degrees (25).

Silicon oxide can be crystalline or amorphous (as in glass) depending on the environment of its formation. Twenty five percent of earth’s crust is made of silicon, and silicon is the second most abundant element after oxygen. Elemental
silicon is not found in nature, occurring as silicon oxide or silicates. Surfaces of crystalline silicon have become one of the most commonly investigated surfaces, and these investigations relate both to the relatively new fields of nano-science and semiconductor electrochemistry and to the more established field of microelectronic device development.

In this study, for the purposes of mechanistic discussion, we assume that the product of anodization has the molecular formula SiO$_2$. The Figure 1.6 below presents the ideal quartz crystal (SiO$_2$) structure. The silicon dioxide produced by anodization is unlikely to be as homogeneous and organized as this representation. It is assumed to be amorphous. Table 1.3 below lists a number of different thermal and anodic oxides of silicon and indicates the variations in O:Si ratios, densities, and other material/electrical/optical properties reported in the literature.

Figure 1.6: Silicon Dioxide (quartz crystal form), blue oxygen, red silicon (25).
Table 1.3: Reported variations in physical properties of anodic silicon oxide (8, ref. 11).

**Hydrogenation of Silicon Surfaces**

The chemical reaction between the silicon surface and HF has been described by Ubara (19) and is shown schematically in Figure 1.7 below.
Mechanism for Silicon Reacting with HF.

Ubara’s (19) mechanistic model of the Si/HF reaction.

**Figure 1.7:** Ubara’s (19) mechanistic model of the Si/HF reaction.

Ubara (19) presented the first explanation for the termination of silicon by hydrogen rather than fluorine when treated with hydrofluoric acid. The silicon-hydrogen and silicon-silicon bond energies are 3-4eV, while that of silicon-fluoride is 6-7eV. Si-F has a higher bond energy which makes it thermodynamically more stable. The above mechanism can be found in Zhang’s book, which referenced Ubara et al.’s paper. (8,8,9). In the intermediate step, silicon is terminated with fluorine.

However the Si-SiF₃ bond is not stable in HF. The Si-Si bond is weakened by the presence of fluorine, and back bonding strongly polarizes the Si-SiF bond (9,9). When HF inserts into this weakened bond, the result is that the silicon surface is terminated with hydrogen.
Mechanisms of Photoreactivity of H-terminated Si toward 1-dodecene

A UV lamp is used as the source of energy that is required to begin homolytic cleavage of the hydrogen terminated bond from silicon, creating a radical as illustrated in Figure 1.8 (bottom) (20). The radical is highly reactive and reacts with the double bond of the 1-alkene to form a radical on carbon as seen in step two of the mechanism shown in Figure 1.8. The carbon radical then abstracts hydrogen from a nearby silicon, thus creating another silicon radical. A chain reaction continues until all terminal hydrogen has reacted or until the reaction is terminated. As seen in Figure 1.8 (top), if oxygen is still in the organic reagent, a second reaction pathway could occur, in which oxygen competes for the available radical silicon sites, thus forming unwanted oxide.

*Photoreactivity of H-Si(111)*

![Figure 1.8: Representation of mechanism for the photochemical reaction of (top) silicon $<$111$>$ with O$_2$ and (bottom) silicon $<$111$>$ with 1-alkene (20).](image)
2. Materials and Methods

General Notes on Silicon Surface Processing

As stated above, these studies begin with crystalline silicon wafers with a thin native oxide layer. This native oxide layer spontaneously grows in humid air to thicknesses that range from 0.2 nm (after minutes) to 3 nm after days of exposure. To the environment (8, p65, ref.28). Native oxide grows at a somewhat slower rate for hydrogen-terminated (see below for method of H termination) Si as compared to a freshly cleaved silicon crystal surface (8). Perhaps the most important assertion for us regarding native oxide that appears in the literature is that of Dagata (14) where he states that the rate of native oxide growth after hydrogen termination is slow enough that it may be disregarded when carrying out anodic oxidation with AFM (for experiments occurring within hours of surface preparation). For this reason, it will be assumed that H-terminated surfaces can be considered to remain H-terminated throughout an afternoon of experimentation. Both Si and SiO₂ are insoluble in water. While SiO₂ is soluble in HF, Si is not.

Fabrication Environment

Most semiconductor based device fabrication is carried out in a clean room environment, a rather large and high cost environment not available at MU or at many other university research facilities. Particulates are removed from the air in a clean room using either HEPA filters, which are designed to remove particles larger than .3 microns or ULPA (ultra low penetration air) filters to remove particles >.12 microns. The dust filled environment of the MU science building certainly can be
expected to add some variation to the quality of the prepared surfaces, however 
roughness analyses of the materials used (Table 4.1) show that for experimental 
purposes (perhaps not for manufacturing) the MU environment was acceptable. To 
minimize the effects of this ‘dirty’ environment, all Si surfaces were transported in 
1 inch, industry standard wafer carriers (natural polypropylene). Also, care was 
taken to avoid potential trouble that may arise from contact with dusty bench 
surfaces and equipment.

**Si Wafers as Received**

Commercially available silicon wafers, <100> orientation from Virginia 
Semiconductor, had undergone an extra polishing procedure (called Haze Free by 
manufacturer) to provide surfaces with very low surface roughness (figure 4.1). 
The Si is boron doped $p$-type Silicon ($0.1 – 0.3 \ \Omega cm \sim 10^{17}$ boron atoms / cm$^3$). 
These wafers are shipped with what is known as a native oxide layer that is 
estimated to be 5-20 nm thick (personal correspondence with a Virginia 
Semiconductor representative). These estimates are not in agreement with the 
figures given in reference 8, which shows that the native oxide layer is no more 
than 1 nm after 100,000 seconds (more than one day) and never exceeds 3 nm in all 
the literature reviewed (table 2.10, ref. 8). Starting with a 4 inch diameter, 250 µm 
 thick Si wafer, we diced the wafer, by fracturing using a razor blade, into 1cm 
square pieces. These fracture lines are usually quite straight because the razor 
initiates a fine crack in the wafer and makes it possible to break the wafer along a
crystal plane. The 1 cm silicon dice are blown clean with nitrogen up to 1 minute to get rid of any dust resulting from the cutting process.

**Cleaning and Removal of Organic Contamination**

In order to produce a surface that is free of impurities, a cleaning method adapted from RCA was employed. The RCA method is named after a method developed by the Radio Corporation of America while working with solid state silicon based electronics. The first cleaning step is to sonicate the silicon sample in different solvents to remove organic contaminants which are not chemically bound to the surface. The silicon samples are ultra-sonicated in ethanol, then in acetone and finally in HPLC water, with each cleaning cycle lasting for 5 minutes. The ethanol, absolute, 200 proof, for molecular biology, was supplied by Sigma-Aldrich with grad pro analysis. The HPLC grade acetone was supplied by Fischer-Scientific and the HPLC grade water was supplied by Acros Organics. The sonicator was a Model 50 D, from VWR. The setup used is diagrammed in Figure 2.1 below. HPLC grade reagents were used in order to reduce the possibility of surface contamination.

![Diagram of sonication setup](image_url)

**Figure 2.1:** Apparatus used to sonicate silicon in all three cleaning reagents.
Piranha solution, which is a mixture of sulfuric acid and hydrogen peroxide is used to remove organics which are bound to the surface and also to re-oxidize the silicon surface. The mixture of (50/50, H₂SO₄ / H₂O₂ (hydrogen peroxide is supplied as 30%)) is always freshly prepared to ensure the self-sustained temperature of ~80 °C. This ensures a high reactivity in the cleaning process and during oxidation of the silicon samples. After, oxidation, the sample are rinsed thoroughly with HPLC water.

*Caution: piranha solution (H₂SO₄ / H₂O₂) is very exothermic and reactive with organics; it should be handled with extremely care. Additionally it should be noted that 30% hydrogen peroxide is extremely unstable toward decomposition in the presence of impurities and must be handled with extreme caution (gloves, goggles and splash guard suggested).*

**Hydrogenation of the Silicon Surface**

Silicon samples cleaned by sonication and piranha solution as described above are still covered with a native oxide coating. This film was stripped by etching in 7.2 % HF for 10 minutes. Aldrich supplied the HF with grade Selecti-pure (VLSI grade). After HF etching, the samples were rinsed thoroughly with water HPLC grade water.

*Caution: hydrofluoric acid (HF) is very dangerous. skin contact leads to acute disturbance in mineral physiology. It should be handled with extreme care.*

The atomically rough Hydrogen-Terminated Silicon <100> samples are prepared by a dipping of the oxidized sample into 7.2 % HF until the surface is hydrophobic.
(roughly 1 min). Where noted, a longer, 5 minute dipping process was employed. The samples were then rinsed with HPLC water after this HF etching.

Atomically flat Hydrogen- terminated Si \(<100>\) samples were prepared through a process involving the solvent sonication, followed by piranha, followed by the HF rough etch, followed by piranha re-oxidation, then by further etching in 7.2 % Ammonium Fluoride (NH₄F). The Si \(<100>\) is then rinsed in HPLC water and blown dry with nitrogen. The Si Sample were then placed in a natural polyethylene holder and the holder was covered with aluminum foil to slow the light induced re-oxidation of the silicon surface.

**Preparation of an Organic Monolayer on Silicon**

The method used to prepare alkyl mono-layers covalently bound to silicon is a combination of ideas from several papers (22, 23,24,20). The procedure used, and a representation of the reaction scheme for the reaction of 1-alkene molecules and the hydrogen terminated Si surface are shown schematically in Figure 2.2 below.
It is to be anticipated that the grafted organic monolayer can serve as a stable resist toward the deposition of an array of gold at specific location via electroless deposition. Several papers (8, 20) indicate that the hydrogen terminated surface is not stable and that it re-oxidizes by reacting with environmental oxygen. Using an organic layer resist, local oxidation using SPL will activate the specific region of interest while the organic resist will protect all other regions. The procedure employed began with fracturing a silicon wafer with a razor blade as explained above. The usual cleaning via sonication is followed by steps of HF etching, piranah oxidation, buffered HF etching. The methods of cleaning were kept the same for every experiment. After cleaning the surface, handling and transporting them is very important. Our samples are placed in a polyethylene container and covered with aluminum foil to avoid exposure of the samples to light. Prior to
exposing the hydrogen terminated surface to the 1-alkene, the organic compound is
degassed before used by a method called Freeze-Pump-Thaw degassing. It is
important that the solvent be degassed because any oxygen from the solvent may
compete with the organic compound for surface sites.

The Freeze-Pump-Thaw Degassing process begins with placing several drops of the
1-alkene compound, which in this case is 1-dodecene (CH₂ == CH-(CH₂)₉-CH₃ or
C₁₂ ) into a ca 50 ml Schlenk flask. Making sure that the stopcock is sealed to avoid
air entering, the Schlenk flask is attached to the Schlenk line. The flask is flushed
with nitrogen gas, then the flask is place in liquid nitrogen. Once the solvent is
frozen, the flask is evacuated and the Schlenk flask is raised from the liquid
nitrogen and the solvent is allowed to warm until it melts. After melting the solvent
the process is repeated by placing the Schlenk flask back into liquid nitrogen to
freeze the dodecene inside. This procedure is repeated three to five times for or
until bubbles stop coming out during thaw. After completing this freeze pump-thaw
process, the 1-dodecene is considered to be de-oxygenated. In the next step, the
hydrogen terminated silicon surface is immersed into the 1-dodecene. Following
this, a UV light cross linker is used to illuminate the silicon in the 1-dodecene.

The UV cross linker timer is set to 2350s which is equivalent to approximately 40
minutes. 2350s is the time required to dose the sample with 14 J/cm² of energy
with a lamp which provides 6000 µJ/cm² per second (6000 micro watts / cm²)
power output. According to reference 20, this dose is sufficient to complete this
photoreaction. After 40 min of illumination, 1-alkene-terminated silicon surfaces were obtained. The sample was then rinsed, then sonicated in a methylene chloride, CH₂Cl₂, bath.

Water Contact Angle Measurements

Water contact angle (WCA) measurement determinations were performed for monolayer characterization using Image J software (with plug-in). The shape of a liquid droplet on a surface contains information about the surface. The angle at which a liquid/vapor interface meets the solid surface provides a quantitative measure of hydrophilicity or hydrophobicity. In order to perform these measurements, a 2 ul drop of water was placed on the various surfaces (before lithography experiments) and imaged. The arrangement used to capture the droplet image is provided in Figure 2.3. Image J software from NIH was used to analyze the water contact angle, using an Image J plug-in (free download).
**Figure 2.3:** Diagram of the contact angle measurement system (bottom right), example image (top right). Schematic at top left defines angle theta, the contact angle.

**Lithographic Production of Dots**

Forming anodic oxide dots was performed in order determine the relationship between oxide growth and current, voltage, holding time and surface composition parameters. To approach these questions, a series of lithography experiments were performed.

After completing a number of ‘successful’ dot writing lithography trials without varying parameters, a series of experiments in which exposure time and voltage were varied in order to determine their effects on feature size. Multiple series of dot features were produced by varying exposure time in the following order 3s, 2s,
1s, 03s, 0.2s, 0.1s, 0.2s, 0.3s, 1s, 2s and back up to 3s, with voltage held constant. This experimental design was intended to reduce the possibility that changes in tip geometry caused by the lithography operation were responsible for any observed differences in feature size.

In a similar series of experiments, voltages were varied (.5, 5, 10, 12, 16, 20, 22.5, 25, and 30V) while maintaining a constant holding time. Figure 2.4 diagrams these experiments.

**Figure 2.4:** Diagram of design of oxide dot experiments, (left) size vs. voltage at holding time of 2 seconds and (right) dot size vs holding time at voltage of 12V.

Limitations in obtaining current measurements during oxide dot formation related to data collection rates precluded significant analysis of the current efficiencies.
associated with production of these features. Current measurements were performed using a computer interfaced RadioShack Multitester. The instrument was not ideal, since it has only 1 second time resolution. Limitations in the lithography software limited dwelling on spots to 9 seconds. As dot patterns were created, the current readings were difficult to keep in registration with the lithography. Also, determining volume of oxide formed is much more time consuming and prone to human error than finding volume of line structures (see methods below). Finally, small scale in-homogeneities in the surfaces were believed to contribute to the inconsistency in dot formation across single arrays. An example of such an array of oxide features showing inconsistency in dot formation even when the voltage and holding time were kept constant throughout the formation of the oxide array is shown in Figure 2.5 below. The spot array on the right side of Figure 2.5 serves as the design used in forming the dot array image on the left side of the figure.

![Image](image.png)

**Figure 2.5:** Image displaying inconsistency in dot formation which may result from in-homogeneity in doping or surface quality. At right is the proposed design of the 10x10 array, notice the missing dot features in the image at left.
Lithographic Production of Lines

Drawing oxide lines provided a means of concurrently recording the electron flow during the formation of anodic oxide features. Current measurements were made using a computer interfaced RadioShack Multitester. This instrument provided 1 second time resolution. By drawing lines rather than dots, correlation of current and oxide formation was made easier, many more data points could be acquired per experiment and effects of local variation in the surface chemistry that seemed to prevent consistent dot formation as seen in Figure 2.5 was minimized. The temporal limitation of our system in recording the current which lead to the formation of the nanometer oxide features led us to design a method to keep track of the current at each location within the line.

A procedure similar to that used for oxide dot formation was employed. Instead of dots, anodic oxide lines were drawn on the surfaces of hydrogen terminated silicon, silicon with covalently bound alkene mono-layers and on surfaces with native oxide. The results of the comparison are provided in Chapter 4. An important parameter in the programming of line lithography is the scan speed, which was set in µm/s instead of the holding time used in writing anodic oxide dot type features. The option for setting the voltage is the same as that used in the formation of the anodic oxide dot array. Another advantage of measuring integrated current over a line is that the slow ramp up of the voltage source pulse has less relative contribution to the oxide film formation. A protocol was developed to program
oxide lines. Even when drawing lines as the features of interest, it was found that at times the lines were not easily seen in post lithography analysis. For this reason, lines were always drawn from the top left hand corner to the bottom right hand corner of the scan window and the scan size was kept the same for all experiments pertaining to oxide line formation. In this way, even when the linear features were not visible, it was possible to analyze the appropriate area on the surface (Figure 2.6). Although this protocol leads to small timing and current errors at the ends of the linear features (ramp up and ramp down and operator delay), it was felt that the analysis of the line data minimizes the effects of these errors. The anodic oxide line is formed with the tip potential negative relative to the silicon at a controlled humidity of 16-25% RH. The protocol employed a scan size of 25 microns (25.214 µm is the closest step allowed by the digital set points in the x, y piezo positioning) and a scan rate of 2 Hz and x, y resolution of 256 data points for every experiment. 6 different voltages were used, 10V, 12V, 14V, 16V, 18V, 20V. The lithographic writing speed was set at 1 µm/s meaning that the line was written at that rate while collecting data points (approximately 10 height data points for each second). A total of approximately 362 height data points can be collected in each line. The corresponding electrical data from the ammeter was collected at one second intervals. This method was used for the study of each of the 3 different silicon surfaces. The voltage and scanning speed parameters were set in the LPM software for lithography. After the writing step was completed, the resolution of the scan and the scanning speed is set in the PNI cockpit software in order to record the image data post lithography. Below are details of these lithography methods.
**Figure 2.6:** Screen capture displaying a red line superimposed on an AFM image of the region where an oxide feature is to be analyzed whether or not the line presence is obvious.

**Humidity Control**

Humidity was controlled in the closed AFM chamber. A tube inserted through a hole in the left hand side of the chamber was used to introduce dry nitrogen gas into the chamber. The chamber was flushed with nitrogen to lower the humidity to a value of relative humidity between 16-25 percent. This allowed imaging experiments to be performed with the lid closed, isolating the scanner from the
environment, while also controlling the humidity during an experiment. All experiments were carried out at RH between 16 and 25%.

**Surface Imaging with Acquisition software (PNI cockpit)**

Prior to a lithographic experiment, the surface is first scanned using the acquisition software (PNI cockpit), and the image is saved as a file. The settings are first set, and the cantilever is brought near the silicon surface. There are several options under the scanner control in the SPM Cockpit™ software, allowing one to set the scan size in µm, the scan rate in Hz, the resolution and scan angle. In a typical imaging experiment, a scan size of ~25 µm, 2Hz and 256 resolution was selected. The tip was approached to the surface (to achieve feedback) and a pre-litho scan within the 25 micron region was performed to provide a topographic image of the surface. The tip is programmed to move in the \( x, y \) plane of the substrate, but responds to follow the topography in \( z \). The first image was saved before lithography performed to allow comparison of the region before and after the lithography experiment. There are problems, including drifting and offset caused by the \( x, y \) piezo (usually temperature) and the displayed image often shows that the substrate has moved during scanning. The observed drift in corner-to-corner experiment was never found to be more than 1 micron in \( x \) and \( y \), and typically was less than 20 nanometer. After the image was saved, the LPM software was opened in order to perform the next step of the experiment.
Lithography via LPM software

A sample was placed in a sample holder for the AFM. The LPM software was opened and programmed with scan speed kept at 1 µm/s, while varying the voltages for each experiment. As shown in Figure 2.7, an EMCO model C01 (EMCO, Sutter Creek, CA) DC amplifier (multiplier) was connected to the output of the PNI system. This multiplier has an output range of 0-100 volts that is linearly related to a 0-5 volt input control voltage. The image scanned from the acquisition program is opened using the LPM software. The software has an option of either creating an array of dots or drawing lines on this image. The voltage to be applied to the surface is set. Prior to applying the voltage the programmed line is then drawn over the image where it will be executed. The system was configured to simultaneously collect current data while performing lithography on the surface of the material. The importance of this is that it allows one to collect current readings and match these readings (1 second interval) to approximately 10 data Z (height) points within the line per each second of lithography. That information is useful in determining the relationship between the oxide growth and the amount of electrons used at each location. Note that while the AFM tip is grounded the voltage is directly applied to the sample. In order to determine the amount of current passing through the circuit, the ammeter was incorporated into the circuit in series. Note: A test of the circuit is always performed prior to performing any lithography experiments. The voltage in and the voltage out are verified in order to make certain that the exact desired bias is being applied.
Current Monitoring During Lithography

For current monitoring, an ammeter program is opened on the AFM computer and a file is created to save all of the current readings relevant to the writing experiment. The lithography and the ammeter logging program are started simultaneously. The line displayed on the monitor changes color, reflecting the progression of the lithography experiment. When the LPM stops, the ammeter logging program is stopped manually, and the current readings are save to a file. The next step is to go back to the acquisition software (PNI cockpit).
**Post Lithography Imaging**

A second image is acquired at the same location, by clicking the scan icon. The line can sometimes be seen while an image is being acquired, depending on the amount of voltage applied for that particular lithography experiment. The tip stays in contact at all times, and ideally an image is capture of the same region for analysis. This captured image is called the raw data image. This image is then saved until it is next further processed in NanoRule software where all analysis of collected data is performed. When saving images, the software will ask to save the image with or without leveling. It is suggested that one always chose the option of save without leveling, so that leveling can be performed in the NanoRule software. The Raw data image is opened as a PNI file. In Chapter 3 below, an example is provided of the process used to determine the oxide volume by using the functions available in the NanoRule software.

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**3. Data analysis**

**Processing Images of Oxide Dots Using PNI NanoRule Software (21)**

The determination of the height of the anodic oxide provides insight into the mechanism of oxide film growth. Data is recorded as z-height, making AFM an ideal tool to measure this height. A method was defined for analyzing the anodic oxide dots. As an example, the analysis of the dot shown below in Figure 3.1 is described below. The first step when processing image data using NanoRule
topography software is to upload a file saved using the acquisition software (PNI cockpit). The nanometer scale features are not usually visible in the raw data file, because of the tilt in the image, especially if working in a 1-5nm (z) range. The software has tools that can be used to process and enhance the image’s view by rescaling, normalizing or filtering of the raw data. Within the processing menu there are several icons, which include leveling, histogram, filter, zoom to scale, error correction and rotation. For this particular experiment of the oxide dots, 2 of these functions were employed, leveling and zoom & scale. Sometimes the error correction is used in cases where a strong feature, which is either not part of the surface (an artifact) or a real feature which would interfere with the result, are unnecessary components of the image. Error correction enables one to erase an artifact in order to emphasize the feature of interest. An example source of artifacts would be momentary electronic problems or a vibration that leads to scan line jumps. The first icon used brings up the leveling function. There are several orders of leveling to choose from. Generally the 1st order polynomial is used. This removes the tilt from an image as discussed above. There are also two options of dimension to choose from, and the one dimension, horizontal one is used. As data leveling is necessary to observe small features, this is the first step to perform all the time when processing the oxide data. The next function to use is zoom to scale, (select icon, or select process → zoom to scale… to open the tool). Once the tool is open one selects resolution and data point ranges (areas). Consider the oxide dot image in which an array of 12 x 10 anodic oxide dots had been written, each with a related holding time. Holding time for each dot starting from left to right for every
row is 3s, 2s, 1s, 0.3s, 0.2s, 0.1s, 0.2s, 0.3s, 1s, 2s, and 3s. This holding time pattern is repeated for every row. Each oxide dot is analyzed separately from the rest of the oxide dots by zooming to the location of the dot and choosing the 64x64 pixel resolution so that the region is over sampled (~30 x 30 data points). This method is repeated for every dot separately to obtain the relative height in nanometers. Once these options are selected for each oxide feature, the analysis tools are used. The analysis tool menu has a list of tools to be use for analysis. There are several analysis menus that can be used to define and measure lines and regions within the image. Analysis tools available in the NanoRule software are Line and Angle, Roughness, Step height measurement, Power spectral density and DVD analysis. For this set of experiments the Line and Angle measurement tools are used when studying oxide features. Roughness measurements were also made when obtaining the surface roughness and root mean square roughness of the surfaces before lithography. Once an image region which has only one oxide feature zoomed in with resolution of 64 x 64 is obtained, the Line & Angle analysis menu (click icon or select Analysis → Line and Angle Analysis to open the tool) tool can be opened. Within this tool there are three options of the line orientations, which are horizontal, vertical, and variable. There is also a line width area which allows one to choose a number that best suits the study. According to the NanoRule software, “the line width determines the number of pixels near the selected point that will be averaged to define the height data at that point” (16). This reduces the effect of pixel to pixel variation within a local region on the measurement. For these experiments, a line width of 10 was used for every oxide dot measurement.
Height measurements were taken in 4 directions, which include horizontal, vertical, diagonal from left corner to right, and diagonal from right to left as demonstrated in Figure 3.1. The average of all those heights was taken as the representative oxide height, the plot of holding time vs. height is shown in the results section. This protocol was used to minimize operator variability when quantifying topography thus allowing one to draw conclusions about the relationship between height and experimental parameters. As described below, the growth of height with increasing holding time and voltages was observed.

**Figure 3.1:** Screen captures illustrating method of measuring and averaging dot height in obtained from four different line sections.
Processing Images of Line Oxide Using PNI NanoRule Software

As explained in the section of oxide dot formation, the height and volume of oxide are of interest in these experiments. The method of determining the height of the line of anodic oxide is described in this section. The data saved in the acquisition software (PNI cockpit) is uploaded for further analysis. As mentioned before, the raw data must be leveled to remove tilt. When leveling this image a horizontal one dimension leveling is chosen. The same 1\textsuperscript{st} order polynomial as used when processing the anodic dot oxide is employed. The next step is different. The zoom to scale step is skipped and the Analysis tools, Line and Angle is opened. Within this tool, the variable option is chosen because it allows the line to be drawn in any direction. A line width of 4 data points is selected, and the analysis line is drawn on the line from the top left hand corner to the bottom right hand corner. The drawn line appears as a red line (Figure 2.6), which makes it easy to visualize as the line is drawn on top of the actual anodic oxide line.

Clicking on the export command from that menu and saving it as an xls type file allows the analysis of all of the height data collected within the line. The data appears in two columns of approximately 350 data points. The first set is for the location in microns (xy plane) and the second set is the \( z \) height in nanometers. The 350 data points of distance/height information are divided into 1 second intervals and associated with ammeter readings. After these data has been exported to Microsoft Excel, another line is drawn, however this time the line is drawn next to the oxide feature. This provides a background to subtract from the region with the oxide to give a difference which is the actual oxide feature height. In order to
minimize the influence of noise in the data, ~10 height data points will be binned and associated with each current reading collected from the ammeter.

Figure 3.2: Screen capture of the zoom/scale function used in the determination of the oxide volume from sub region of a lithographically drawn line.

This time a Zoom and Scale icon is selected. As can be seen in Figure 3.2 above, a resolution and data point of 64 x 64 was chosen for this particular zoom and scale process. In order to normalize for variation along the oxide lines three different regions of each line were zoomed and scaled and analyzed. The first region analyzed is labeled top in Figure 3.2, when that is finished, data is collected from the region labeled middle and finally data is collected from the region at the bottom.
Once the zoomed, selected region image is displayed at the 64 x 64 pixel resolution, the image is rotated by clicking on the icon called rotation. The image is rotated by 45° and the oxide line will then appear in the middle of the image and it will be oriented vertically. Next the leveling function is invoked using the leveling icon. 3 point leveling is selected since the now relatively large feature would produce undesired effects if horizontal line leveling was employed.

Figure 3.3: Screen capture indicating the method for obtaining the cross sectional area of an oxide line using NanoRule software.

After 3 point leveling is performed, the analysis menu is used to export height information to Microsoft Excel. This time horizontal line orientation of 50 line
width (smoothest averaging available) is chosen from the menu (where the letter A is seen in Figure 3.3). Also within the display option, still in region A of Figure 3.3, the software option is invoked to average all three lines that are to be drawn (see location B in Figure 3.3). The “markers” icon is also checked, in order to be able to designate the location in the image on the topography plot where the cross section of the oxide line starts and terminates. In region C of the top screen capture in Figure 3.3, a line profile plot with two parallel red vertical lines is displayed. The distance coordinates of those two parallel lines on the plot can be traced back to the coordinates of the red X’s in the top image region of the display in Figure 3.3. All the height (in nm) and the location (in µm) are averaged and displayed in location D of Figure 3.3. Once the line analysis of the oxide line region is performed, the screen is captured and saved, since it contains information about the height and the location of the oxide line. In order to export all of the line plot data for region C to Microsoft Excel, one must click the right mouse and the menu seen in the top screen capture of Figure 3.3 is displayed, and “export” is selected. The file is saved as an Excel file. Location D in the top screen capture part of Figure 3.3 above has values of the coordinates and the calculated difference in height between the designated points. Although all of the cross section data was exported to the Excel file, the values for regions outside of the oxide line region designated (demarked) by the markers (red X’s) is considered background. The method used to extract the line height and to obtain the volume of the oxide line is described below.
As an example of how this data was processed, consider for example a 10 point set of paired data, one coordinate is for the location in microns along a line perpendicular to the oxide line. The other coordinate set is the height data. Each height is paired with each location to correlate $x$ and $z$ in the line profile. The average apparent height of the oxide line, is calculated by averaging the $z$ data for all data points with coordinates demarked by the two lines designated in region $C$ of Figure 3.3. A height average is also made for the coordinates outside of the selected region, since this represents the background height. Subtraction of this background from the apparent oxide line height provides the actual height of interest. For example, for the 10 point data set, if points 4 and 9 represent the $x$ and $z$ coordinates of the surface at the sides of the oxide feature, and thus the background, then the height of 4 and 9 is to be averaged. Then the average height from locations 5 through 8 are averaged. Then the average of height in location 4 and 9 is subtracted from the average of the heights of locations 5 through 8. This produces an average height of the oxide line. This procedure should reduce bias introduced by the researcher. The area of the cross section of the oxide line (in nm$^2$) is the product of the average oxide height and the oxide line width, which is the difference in the $x$ coordinates of the two parallel lines seen in Figure 3.3. This area is then multiplied by 35000 nm (35 micron line length) to obtain the line volume above the surface. This value is then further multiplied by two which is assumed to provide the actual oxide volume formed. The factor of two derives from the assumption that the depth profile of the oxide feature is the same as the height profile. As silicon oxidizes, the oxide forms both below the surface and above the surface. The
volume of a mole of SiOx is approximately twice that of Si. Preliminary measurements based on etch pit studies (see Figure 3.4) are consistent with the relative contribution of the sub-surface oxide 2x factor used here in the analysis of the data.

The volume obtained from measurements made on the top, middle and bottom regions were averaged. The average volume of the oxide was then matched with the voltage that was applied during lithography. These analyses were performed for experiments with 10V, 12V, 14V, 18V and 20V writing potentials, while keeping the scan rate at 1µm/s. All surfaces (silicon with native oxide surface, silicon with monolayer and hydrogen-terminated surface) were treated identically, and the drawn lines were analyzed in this manner to draw conclusions pertaining to growth of the oxide with voltage.

![Figure 3.4: AFM images of (left image) oxide dots formed on silicon and (right image) pits formed by HF etching of the anodic oxide.](image)

Oxide height features of average 0.729 nm
Indentation showing pits of 0.536 nm
4. RESULTS AND DISCUSSION

Surface Roughness of various surfaces

The Si wafers from Virginia Semiconductor have undergone their haze free treatment. This treatment is quite expensive ($25-30 per wafer) and involves use of polishing devices, fine grit, and solvent cleaning. The details of the process are not shared freely by the company and as can be seen from the roughness data in Table 4.1 and Figure 4.1, the product displays less than 5 angstrom nominal roughness. Also seen in the data table and graph is that the process of H-termination has added roughness to the surfaces.

Two explanations for this may be proposed,

1- Treatment of the surface in the MU, non-clean room environment may have contributed surface particulates, resulting in increased roughness.

2- Steps and terraces may have formed during the HF treatment which were not completely removed by the NH₄F treatment.

The organic mono-layer appears to restore the surface quality. The flexible nature of this surface may enable it to backfill the defects. The results presented in Figure 4.1 and Table 4.1 indicates that shows surface roughness of all three surfaces, with hydrogen terminated with the highest roughness of the three surfaces studied. Starting with the low roughness native oxide, surface roughness increases in the process of terminating the surface with hydrogen (etching the SiO₂ with HF and etching Si-H with NH₄F) and smoothness is recovered with dodecene treatment.
**Figure 4.1:** Root mean square and roughness averages associated with the three different types of surfaces studied.

<table>
<thead>
<tr>
<th>Silicon surface types</th>
<th>Averages</th>
<th>Root mean square</th>
</tr>
</thead>
<tbody>
<tr>
<td>H-Terminated Surface</td>
<td>0.61nm</td>
<td>0.78nm</td>
</tr>
<tr>
<td>Dodecene surface</td>
<td>0.39nm</td>
<td>0.48nm</td>
</tr>
<tr>
<td>Native oxide surface</td>
<td>0.28nm</td>
<td>0.22nm</td>
</tr>
</tbody>
</table>

**Table 4.1:** AFM determined average roughness and rms roughness for the three surfaces studied.
Water contact angle measurement (WCA)

The WCA was determined for each of the three different types of surfaces. Qualitative differences are apparent in the images presented in Figure 4.2 through observable differences in the shapes of the drops on various surfaces. Quantitative values derived from similar images, using Image J software is provided in Table 4.2. The native oxide surface has a lower contact angle and is termed relatively hydrophilic. The water spreads out thus resulting in a small angle of contact. The H terminated surface demonstrates a much higher contact angle which indicates an intermediate hydrophilicity. The organic monolayer shows the highest water contact angle. The non-polar tails of dodecane are more hydrophobic than the hydrogen terminated surface. It should be noted that substrates used for WCA measurements were not used for downstream chemistry. Instead, extra Si chips were prepared in parallel with the experimental chips in order to avoid complications that may be caused by exposure to water, light and the atmosphere during WCA measurements. Surfaces of higher hydrophilicity can be expected to form a larger water meniscus at the tip (see discussion of Figure 4.13 below).
Example water contact angle measurements

<table>
<thead>
<tr>
<th>Surface Type</th>
<th>Contact Angle (degrees)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Native oxide layer on Si</td>
<td>63.545</td>
</tr>
<tr>
<td>H-Terminated Si Surface</td>
<td>83.252</td>
</tr>
<tr>
<td>Alkane monolayer on Si</td>
<td>88.263</td>
</tr>
</tbody>
</table>

Figure 4.2: Example images of water droplets on prepared surfaces, the Image J software interface and measured contact angles.

Table 4.2: Contact angle data and average value of the contact angle for the three types of surfaces.

<table>
<thead>
<tr>
<th>Trial</th>
<th>Native Oxide</th>
<th>H-Terminated Silicon</th>
<th>Alkane-monolayer</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>63.545</td>
<td>83.252</td>
<td>88.263</td>
</tr>
<tr>
<td>2</td>
<td>60.238</td>
<td>88.079</td>
<td>90.213</td>
</tr>
<tr>
<td>3</td>
<td>66.004</td>
<td>85.443</td>
<td>90.417</td>
</tr>
<tr>
<td>4</td>
<td>57.982</td>
<td>83.287</td>
<td>87.266</td>
</tr>
<tr>
<td>average</td>
<td>61.942</td>
<td>85.015</td>
<td>89.040</td>
</tr>
</tbody>
</table>

Dot Shaped Oxide Features

Figure 4.3 presents examples of AFM images of oxide dots structures produced on the various generated in this study. Hundreds of such experiments, each taking ~ 1 hour to complete (not including analysis), were performed.
Figure 4.3: Example AFM images of oxide patterns written on different silicon surfaces produced in this study.

The initial goal was to make patterned substrates to act as scaffolding for DNA based nano-arrays. Figure 4.4 provides an AFM image of an early successful efforts to make micro patterned substrates. Although the pattern is SiO$_2$, not gold or platinum, the intended 5 and 6 micron spacing of features required in the scaffolding design was achieved.
Figure 4.4: AFM image of organic monolayer with oxide dot pattern (20V, 2sec hold time per dot). This is proposed anchor sites for one end of director strand only.

After realizing that anodic oxidation rather than field induced deposition of gold was occurring, effort was focused on making a detailed study of silicon oxidation with SPM.

Dependence of oxide height on voltage at constant holding time.

A marked dependence of oxide height on bias voltage was observed. The example AFM image and data graphed in Figure 4.5 represent results obtained for the H-terminated silicon surface with oxide dots formed as the voltage was varied from
2.5V to 30V at dwell time of 2 seconds. There is a noticeable increase in the dependence of the oxide height on voltage at higher voltages.

Figure 4.5: Oxide thickness dependence on voltage, (left) AFM image of example oxide dot results and (right) graph of experimentally determined dependence (averaging several trials).

The spot diameter also appears to increase with higher voltages, producing bigger spots. Note the approximately exponential increase in oxide growth at higher voltage seen in the graph in Figure 4.5. The highest oxide height is observed at 30V while the smallest is not easily visible at 2.5V. Oxide growth was not characterized above 30V because it was observed that this high voltage removes the aluminum back coating on the tip, thus causing the laser to deflect everywhere and breaking the feedback loop that maintains tip contact.
Note: Any deflection of the cantilever when it raster scans on the surface is detected on the photodiode. The aluminum coating serves as a mirror to make the laser deflect on contact with the sample.

**Dependence of oxide height on holding time at constant voltage.**

Figure 4.6 presents results obtained during experiments in which an array of 12 x10 oxide dots were prepared at different dwell times while maintaining a constant bias voltage of 12V. The oxide dot height is plotted versus holding time. For this set of experiments, the holding times used starting from the left to the right were 3s, 2s, 1s, 0.3s, 0.2s, 0.1s, 0.1s, 0.2s, 0.3s, 1s, 2s and 3s. Each row of the array had the holding time varied in the same manner to produce the oxide dots. As seen in Figure 4.6, there is a strong dependence of feature height on holding time at sub-1 second times. However, there appears to be a threshold above which holding time has little effect on feature height. This is likely due to diffusional limitations within the oxide, however other potential mechanisms limiting growth may involve stress buildup, field breakdown or even water consumption. Because current measurements were not taken for these oxide growth experiments, the relevance of the field induced breakdown cannot be determined. It is possible that water is consumed (15). This point is very relevant to the design of reproducible methods of forming spots at each location.
Analyzing electrochemical efficiency and performance using linear structures

Although all three surfaces were successfully patterned with oxide dot features, in some experiments it was noticed that some expected dots were missing. This inconsistency in oxide dot formation is believed to result from in-homogeneity in doping or surface quality, such as variations in dopant concentrations, steps and kink sites. These preliminary results led to an investigation of the electrochemical efficiency of the system, a divergence from the focus on the direct application of SPL to DNA based nano-array technology to the study of nano-lithographic anodic oxidation.

As described above, making useful current measurements that were aligned in time with the lithography was difficult with dots. Quantitative studies required a switch to drawing and recording data during fabrication of a single, diagonal oxide line.
Examples of line features made at Marshall University are shown in Figure 4.7 below.

**Figure 4.7:** Example AFM images of oxide lines drawn at various potentials while simultaneously recording the electrical current.
**Resistance of system at tip/substrate interface**

![Diagram](image)

**Figure: 4.8:** Diagram indicating distribution of resistances in the SPL system. Note the junction at the tip/substrate interface.

In any electrical circuit, including the one diagrammed in Figure 4.8, the same amount of current passes through each part of the circuit. The point of greatest interest here is the resistance that occurs at the tip sample interface. To use the obtained current and voltage experimental data to approximate this value, all other sources of resistance in the system must be identified and considered. It was concluded that the resistance of the wires and the metal coating were all \( \sim 0 \) \( \Omega \), while the resistances at the surface and tip were also considered negligible (on the order of 200 \( \Omega \), see Figure 4.9 for estimations of resistance in sample and probe). Figure 4.10 presents the current-voltage data used to calculate the resistance at the tip/sample interface.
Figure 4.9: Approximations used in determining the non-interfacial resistances in the Si parts of the lithographic system.
Voltage vs. Current (After breakdown)

**Figure 4.10:** Graphs (upper row) displaying current vs voltage dependency in the high current regime (this study, uA), and (lower row) result from (4) showing both low (nA) and high (uA) currents during oxidation.

Figure 4.10 presents the average currents calculated for each voltage used in writing oxide lines on native, hydrogen-terminated and organic monolayer silicon surfaces. Using the known current and voltage in each case, a resistance at the tip interface can be calculated. This resistance was found to be different for every surface. The resistance of the native oxide was found to average $R = \sim 83k\Omega$, for hydrogen terminated it was determined to be $R = \sim 62k$ and the dodecene monolayer resistance was found to be $R = \sim 19k\Omega$. In this determination the trend lines (see Figure 4.10 top row of plots) were not forced through zero/zero relationship for the different surfaces. The y intercept value for these trend lines was ignored because the lines may cross the y axis near the breakdown voltage. Therefore
(in the low current regime) a different trend line would be expected to fit the low current data. The last two graphs at the bottom of Figure 4.10 present data obtained by Lyuksyutov, and indicate that only nanoamps of current passed when the voltage is in the low current region. Note that the equation that fits the trend is quite different in this low current regime (4).

Figure 4.11 presents plots the calculated number of moles of SiO₂ formed during a lithography experiment against the voltage applied during line writing. The error bars reflect the difficulty in making these determinations. The only trend with significant reproducibility was the one observed for the h-terminated surface.

**Figure: 4.11** Graphical representation of the dependence of the number of moles of silicon oxide formed on voltage for each of the different surfaces studied.
Surfaces showing noticeable failure to mark a trend were the native oxide and the
dodecane coated surfaces. Although a trend was not observed for the native oxide, it
was noticed that the overall oxide growth was higher on this surface than on the
other two surfaces, hydrogen terminated and organic terminated (see Figure 4.13
below).

![Figure 4.12: Efficiency relationships from all surfaces.](image)

In Figure 4.12, a noticeable relationship of efficiency with applied voltage is
observed for both the hydrogen terminated and for the organic monolayer surfaces,
while the native oxide shows no trend. In the case of the hydrogen terminated silicon surface, additional potential applied yields added chemical change. In the case of the organic terminated silicon surface, the added voltage causes higher current but decreased chemical efficiency. Ionic efficiency is expressed as the number of moles of silicon oxide generated for every 4 moles of electrons consumed. In a Faradaic electrochemical system, “The number of electrons that cross an interface is related stoichiometrically to the extent of the chemical reaction” (9), which means that the amount of electrons consumed is related as a reactant to the molecules of silicon oxide formed. This is clearly not the case for any of the surfaces studied here, at the potentials employed.

There are two types of charge transport effects which may partially account for the decrease in dodecene electrochemical efficiency with increasing voltage; 1- electrons are passing as current through an additional dodecene induced conduction mode 2- the dodecene itself may interfere with the formation of the oxide by consuming some of the current as an oxidation product.

An important observation, presented graphically in Figure 4.13, is that the measured contact angle is inversely related to the number of moles of oxide produced (these are the 16V and 18V experiments from each surface, more data was available for these groups).
Figure 4.13: Contact angle (top) and moles of oxide produced (bottom) on various surfaces. In the middle is a hypothetical diagram of the tip sample interface including the water bridge.

One possible explanation for the generation of more silicon oxide on the native oxide surface as compared to the other silicon surfaces is provided by the relationship with the water contact angle measurements. A consideration of the contact angle and growth data presented in F 4.13 reveals that growth decreases with increasing hydrophobicity of the surface. It would appear that hydrophilic
surfaces create a greater surface area of water, and this results in a larger path for current carrying electrolyte species to reach the surface to generate oxide features.

![Figure 4.14](image)

**Figure 4.14:** Ionic efficiency (a) and resistance (b) compared.

As seen in Figure 4.14, ionic efficiency increases with increasing resistance. This may reflect parsing of the current between ionic currents, which build up the oxide, and electronic currents, which may not be electrochemically active. I.e in the low current regime, only ionic species are responsible for carrying current through the gap, thus promoting redox reaction. In the high current regime, more current carrying species in the electrolyte are produced by the field breakdown and those includes protons, electrons, hydroxyl, and radical species (4).
**Conclusion**

The generation of the anodic oxide is the result of the two obvious reactants, which are the silicon wafer and water, in the presence of the applied voltage. There are at least two mechanisms found in the literature whereby silicon and water can combine. Water in the presence of high field is reduced (4) by electrons emitted from a negatively bias tip. The field will then assist in the transportation of oxyanions (O-, OH-) through the oxide. This field also reduces the effects of the stress which results in the mismatch of volume between the Si and SiO₂ (15). Evidence of gross physical changes has been observed in this study, at surfaces at high voltage (>25V). The mechanisms of these changes are unknown. Faradaic (ionic) current predominates at low voltages and decreases as oxide builds in constant voltage mode (8). The instrumentation used in these studies should be able to maintain constant voltage under the regimes studied. The voltage multiplier is rated at 10mA output so the voltage should not be compromised even at the relatively high currents (microamp) observed in this system. The oxidized Si features do not exceed nanometers in thickness, therefore capacitive breakdown (mA and μA current flow) is highly probable, with a field strength approaching ~ >1⁰⁹ V/cm based on 1 angstrom tip/sample distance anticipated for contact mode writing. The efficiencies observed are less than 0.00000001% efficient in the high current regime. A method has been described in detail for the production of self limiting oxide surface features.
On the practical side, this effort has led to the production of a modified AFM system capable of producing uniform arrays pits on a very flat surface. An example of a 10x 10 silicon oxide dot and silicon pit array is presented in Figure 4.15 below.

![Figure 4.15: Images of silicon wafer showing the oxide features prior to treatment with HF (left), and pits after exposed to HF (right) (top row); (bottom row) Schematic of the fabrication process.](image)

The future holds a great deal of promises, and it is often not immediately clear what the terminal value of any research endeavor is.
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